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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

WALLACE, SCOTT A

ART UNIT PAPER NUMBER

2671

DATE MAILED: 02/12/2004

17

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/813,035

Applicant(s)

ASANO, MASANARI

Examiner

Scott Wallace

Art Unit

2671

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 November 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments filed 11/20/03 for claims 1-11 and 15-16 have been fully considered but they are not persuasive. The applicant argues on pg 12, 1st paragraph that "Sherburne merely teaches carrying out fixedly the bit conversion from input to output, which differs from the area adjustment circuit of the present application, which is adapted to write data having a width adjusted with an additional area taken into account". Claim 1 does not mention the width is adjusted. However, Sherburne teaches changing the size of the memory depending on the size of the image data and overlay data in column 5 lines 55-67 and fig 7c.
2. On page 13 the applicant argues that "Sherburne does not provide adequate support for the implied relationship between the circuits. Particularly, the ground for the area adjustment circuit is presumed and not logically supported". As seen above, Sherburne discloses adjusting the area of the memory, which is what the area adjustment circuit does. There is no difference if one circuit does the claimed features or a separate circuit does each one separately. The functions still get done.
3. The applicant also argues that Sherburne fails to disclose "that the additional data are written in with the additional area's address". It was well known to store data in memory at address locations to better organize the data.
4. Applicant's arguments with respect to claims 12-15 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Knox et al., U.S. Patent No. 6,175,388 in view of Tamura, U.S. Patent No. 6,233,658.

7. As per claim 12, Knox et al discloses an image processing method (column 2 lines 56-60) comprising the steps of: setting up, in a storage circuit in which image data is stored (column 3 lines 5-11), a range of an image area in which the image data is written and a range of an additional area which is adjacent to the image area and in which data other than the image data is written (column 3 lines 5-11), with information supplied to a memory space of said storage circuit as a parameter (column 29-43); writing the additional data other than the image data from external into the additional area in said storage circuit (column 3 lines 20-33); wherein the additional data are written in with an address of the additional area (the use of addresses when storing data was well known to be able to quickly find saved data). Knox et al does not specifically disclose writing the image data at an address location if the image area in said storage circuit according to a second write control signal and writing the additional data with a first write control signal and reading out the additional data stored in the additional area and the image data stored in the image area in said storage circuit in response to a first read control signal. This is disclosed in Tamura in column 1 lines 35-51). It would have been obvious to one of ordinary skill in the art at the time the invention was made to read data concurrently because Knox is displaying the OSD data along with an image because this would save processing time instead of using two read controls, only one is needed because the data is being displayed at the same time.

8. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Knox et al in view of Tamura in further in view of Intihar, U.S. Patent No. 6,300,964.

9. As per claim 13, Tamura discloses wherein said step of reading out the additional data comprises the steps of: reading out the additional data from the additional area in said storage circuit in response to

the first read control signal (column 1 lines 35-51). However, neither Tamura or Knox discloses reading out the image data from the image area in said storage circuit in response to a second read control signal. This is disclosed in Intihar in the abstract. It would have been obvious to one of ordinary skill in the art at the time the invention was made to read using separate control signals because this would allow the certain data to be displayed instead of everthing.

10. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Knox et al in view of Tamura in further in view of Bilbrey et al., U.S. Patent No. 5,227,863.

11. As per claim 14, Knox and Tamura fail to disclose wherein the first write control signal and the read control signal are a transfer enable signal enabling an execution of processing. This is disclosed in Bilbrey et al in column 8 lines 43-65. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the read and write signals transfer enabled to execute processing because the data is being displayed therefore the read would have to be processed to be displayed.

12. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Knox et al in view of Tamaura in further in view of Choi et al., U.S. Patent No. 5,673,087.

13. As per claim 15, Knox and Tamura fail to disclose wherein said step of reading out the additional data inserts the additional data read out from the additional area into a predetermined position of a video signal. This is disclosed in Choi et al in fig. 4. It would have been obvious to one of ordinary skill in the art at the time the invention was made to put the additional data in a certain position of a video signal because the user may want the additional data displayed at a certain time.

14. Claims 1-2, 11 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sherburne U.S. Patent No. 5,818,433 in view of Knierim U.S. Patent No. 4,755,810.

15. As per claims 1 and 16, Sherburne discloses an image processor comprising: a storage circuit storing therein image data (column 4 lines 24-40); a data input/output circuit controlling input/output of the image data (column 4 lines 52-55); an access control circuit controlling access of writing in and reading out the image data to and from said storage circuit (column 4 lines 52-55); a memory control circuit comprising an address generation circuit generating an address in said storage circuit to and from which the image data is written in and read out (column 2 lines 17-21), said memory control circuit comprising an area adjustment circuit which sets up an additional area adjacent to an area in which the image data is actually stored in a memory space of said storage circuit and storing therein data other than the image data (abstract and column 2 lines 29-47), which adjusts the address generated by said address generation circuit, and which reads out the image data from said storage circuit, including the data in the additional area, in response to the address and a read control signal supplied to said storage circuit (column 2 lines 17-21). However, Sherburne does not disclose a refresh circuit controlling refreshing of said storage circuit. This is disclosed in Knierim in column 4 lines 24-35. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the refresh circuit of Knierim with the system of Sherburne because this would have kept the screen from flickering.

16. As per claim 2, Sherburne discloses wherein said area adjustment circuit sets up the additional area immediately preceding or following the area in which the image data is stored (column 2 lines 29-45).

17. As per claim 11, Sherburne discloses wherein said access control circuit supplies the data other than the image data to said memory circuit (column 4 lines 52-55).

18. Claims 3, 5-7, 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sherburne in view of Knierim in further in view of Knox et al., U.S. Patent No. 6,175,388.

19. As per claim 3, the combination of Sherburne and Knierim does not specifically disclose wherein information on a position of the additional area is supplied as setting information included in header information. However, this is disclosed in Knox et al in column 3 lines 39-55. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use this header information in Knox

et al with the systems of Sherburne and Knierim because this allows the OSD bitstream to be modified by the user.

20. As per claims 5-7, the combination of Sherburne and Knierim does not specifically disclose wherein said area adjustment circuit obtains information on a base point in the memory space, a row direction width, and a column direction width and outputs the obtained information to said address generation circuit as a parameter. However, this is disclosed in Knox et al in column 3 lines 29-43. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use this information of Knox et al with the systems of Sherburne and Knierim because this allows the memory for the other data to be adjustable.

21. As per claims 8-10, Knox et al discloses wherein said area adjustment circuit supplies the data, which is read out from the additional area, to a predetermined positional in a video signal (column 32-37).

22. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sherburne in view of Knierim in further in view of Herz et al., U.S. Patent No. 5,883,675.

23. As per claim 4, The systems of Sherburne and Knierim do not specifically disclose wherein said area adjustment circuit sets a size of the additional area using information, which is obtained in synchronization with a supplied vertical synchronization signal, as a parameter and reads out the data stored in the additional area in response to a data transfer request. However, this is disclosed in Herz et al in column 1 lines 13-15. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the vertical synchronization signal in Herz with the systems of Sherburne and Knierim because this is the part where no video data is being sent so other types of data have a chance to be sent.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Scott Wallace** whose telephone number is **703-605-5163**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor,
Mark Zimmerman, can be reached at 703-305-9798.

Any response to this action should be mailed to:


Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA,
Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be
directed to the Technology Center 2600 Customer Service Office whose telephone number is
(703) 306-0377.


MARK ZIMMERMAN
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